UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,689	02/08/2002	Zhong Dong	M-12327 US	2077

7590 12/17/2002

Michael Shenker
SKJERVEN MORRILL MacPHERSON LLP
Suite 700
25 Metro Drive
San Jose, CA 95110-1349

EXAMINER	
PIZARRO CRESPO, MARCOS D	
ART UNIT	PAPER NUMBER
2814	7

DATE MAILED: 12/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/071,689	DONG ET AL.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7 and 10-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7 and 10-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: M-12327 US
Filing Date: 2/8/2002
Claimed Foreign Priority Date: none
Applicant(s): Dong et al.
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment in paper no. 6 filed on 10/29/2002.

Acknowledgment

1. The amendment in paper no. 6 filed on 10/29/2002 in response to the Office action mailed on 8/14/2002 has been entered. The present Office action (paper no. 7) is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-3, 7, and 10-29.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 7, and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hagiwara (US 5847427).

4. Hagiwara shows all aspects of the instant invention including a method for fabricating an integrated circuit comprising a nonvolatile memory, the method comprising:

- forming a first layer **202** comprising a silicon surface and providing a floating gate for the memory (see, *e.g.*, fig. 10A)
- nitriding the silicon surface of the first layer **202** to incorporate nitrogen atoms into the surface, wherein the nitriding operation comprises ion implantation of a material comprising nitrogen into the silicon surface (see, *e.g.*, fig. 10C, col.6/ll.2-6)
- forming at the nitrided surface a first dielectric **203**, wherein forming the first dielectric **203** comprises forming silicon oxide at the nitrided surface (see, e.g., fig. 10C, col.7/ll.42-58)
- forming a conductive layer **204** separated from the nitrided surface by the first dielectric **203**, the conductive layer **204** providing one control gate for the memory

5. Regarding claim 3, Hagiwara shows (see, *e.g.*, fig. 14) that the silicon surface of the first layer is a polysilicon surface.

6. Regarding claim 7, Hagiwara shows a method of manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

- forming a first layer **202** providing one floating gate for the memory
- forming a first dielectric **203** on a surface of the first layer **202**, wherein the first dielectric comprises a first surface comprising silicon oxide (col.7/ll.42-58)
- nitriding the first surface of the first dielectric **203** to incorporate nitrogen atoms into the first surface, wherein the nitriding operation comprises ion implantation of a material comprising nitrogen into the first surface (col.7/ll.59-62)

- forming a conductive layer **204** on the nitrided first surface of the first dielectric **203**, the conductive layer **204** providing one or more control gates for the memory

7. Regarding claim 10, Hagiwara shows (see, *e.g.*, fig. 13) that forming the first dielectric **203** further comprises:

- forming the first dielectric **203** to have a silicon oxide surface (col.7/ll.42-58)
- nitriding the silicon oxide surface of the first dielectric to incorporate nitrogen atoms into the silicon oxide surface (col.7/ll.42-58)

8. Regarding claim 11, Hagiwara (col.7/ll.59-62) shows that nitriding the silicon oxide surface further comprises ion implantation of a material comprising nitrogen into the silicon oxide surface.

9. Regarding claim 12, Hagiwara shows that nitriding the silicon oxide surface comprises generating a plasma comprising nitrogen ions, and exposing the silicon oxide surface to the plasma (col.6/ll.2-6, col.7/ll.42-62).

10. Claims 1, 2, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (US 6127227).

11. Lin shows all aspects of the instant invention including a method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

- forming a first layer **120** comprising a silicon surface and providing a floating gate for the memory (see, *e.g.*, fig. 2A)

- nitriding the silicon surface of the first layer **120** to incorporate nitrogen atoms into the surface, wherein the nitriding operation comprises ion implantation of a material comprising nitrogen into the silicon surface (see, *e.g.*, fig. 2A)
- forming at the nitrided surface a first dielectric **143**, wherein forming the first dielectric **143** comprises forming silicon oxide at the nitrided surface
- forming a conductive layer **150** separated from the nitrided surface by the first dielectric **143**, the conductive layer **150** providing one control gate for the memory

12. Regarding claim 2, Lin (col.4/ll.60) shows that forming the silicon oxide at the nitrided surface further comprises forming the silicon oxide by thermal oxidation.

13. Regarding claim 16, Lin (col.4/ll.66) shows that nitriding the silicon surface results in forming at the silicon surface a layer of nitrided silicon **130** less than 3 nm thick.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

16. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hagiwara in view of Misium (US 6261973).

17. Regarding claim 13, Hagiwara shows most aspects of the instant invention (see paragraphs 4-9 above), except for the step of nitriding the silicon oxide surface comprising remote plasma nitridation.

Misium (col.2/ll.1-4), on the other hand, teaches that remote plasma nitridation is an improved method that does not require a high temperature step for creating a nitrided layer that is resistant to oxide etchants.

It would have been obvious at the time of the invention to one of ordinary skill in the art to nitride Hagiwara's silicon oxide surface by remote plasma nitridation, as suggested by Misium, to lower the thermal budget of the process.

18. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hagiwara in view of Chou (US 6426305).

19. Regarding claim 14, Hagiwara shows most aspects of the instant invention (see paragraphs 4-9 above), except for the step of nitriding the silicon oxide surface comprising decoupled plasma nitridation (DPN).

Chou (col.5/ll.63-67), on the other hand, teaches that nitriding Hagiwara's silicon oxide surface by DPN avoid damages to the surface.

It would have been obvious at the time of the invention to one of ordinary skill in the art to nitride Hagiwara's silicon oxide surface by DPN, as suggested by Chou, to avoid damaging the surface.

20. Claims 15 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagiwara.

21. Regarding claims 15 and 29, Hagiwara shows most aspects of the instant invention (see paragraphs 4-9 above), except for the step of nitriding the silicon oxide surface resulting in a nitrided silicon oxide layer less than 3 nm thick.

Hagiwara (col.6/ll.10), however, shows that an illustrative thickness for such a layer falls between 5 to 10 nm. Although, the claimed thickness (< 3.0 nm) and the prior art thickness (5-10nm) do not overlap, it has been held that a *prima facie* case of obviousness exists where the claimed values and the prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties. It appears that the differences in thickness between Hagiwara and the claimed invention produce no change in the properties of the nitrided silicon oxide layer and therefore would have been obvious (*Titanium Metals Corp of America v. Banner*, 778 F.ed. 775, 227 USPQ 773 (Fed. Cir. 1985)).

22. Claims 17-19, 21, 22, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagiwara in view of Misium and Chou.

23. Hagiwara shows most aspects of the instant invention including a method of manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

- forming a first layer **202** comprising a silicon surface, the first layer providing one floating gate for the memory (see, *e.g.*, fig. 10A)
- nitriding the silicon surface of the first layer **202** to incorporate nitrogen atoms into the silicon surface (see, *e.g.*, fig. 10B)
- forming a first dielectric **203** at the nitrided surface, wherein forming the first dielectric comprises forming silicon oxide at the nitrided surface (see, *e.g.*, fig. 10B, col.7/ll.42-58)
- forming a conductive layer **204** separated from the nitrided surface by the first dielectric **203**, the conductive layer providing one control gate for the memory (see, *e.g.*, fig. 10E)

In addition, Hagiwara (col.7/ll.62-67) teaches that nitriding the silicon surface of the first layer to incorporate nitrogen atoms into the surface may be accomplish by exposing the surface to an atmosphere containing nitrogen-atoms. Hagiwara, however, fails to further specify a remote plasma nitridation (RPN) process or a decoupled plasma nitridation (DPN) process to perform the nitriding step.

Misium (col.2/ll.1-3), on the other hand, teaches that RPN is an improved low-temperature method for creating a nitrided layer that is resistant to oxide etchants, whereas Chou (col.5/ll.63-67) teaches that nitriding Hagiwara's silicon oxide surface by DPN avoid damages to the surface.

It would have been obvious at the time of the invention to one of ordinary skill in the art to nitride Hagiwara's silicon oxide surface by remote plasma nitridation, as suggested by Misium, to lower the thermal budget of the process.

Alternatively, it would have been obvious at the time of the invention to one of ordinary skill in the art to nitride Hagiwara's silicon oxide surface by DPN, as suggested by Chou, to avoid damaging the surface.

24. Regarding claim 21, Hagiwara (col.5/ll.59) shows that the silicon surface is a polysilicon surface.

25. Regarding claim 22, Hagiwara shows the forming the first dielectric further comprises:

- forming the first dielectric **203** to have a silicon oxide surface (col.7/ll.42-58)
- nitriding the silicon oxide surface of the first dielectric to incorporate nitrogen atoms into the silicon oxide surface (col.7/ll.42-58)

26. Regarding claim 23, Hagiwara (col.7/ll.59-62) shows that nitriding the silicon oxide surface may comprise ion implantation of a material comprising nitrogen into the silicon oxide surface.

27. Regarding claim 24, Hagiwara shows that nitriding the silicon oxide surface comprises generating a plasma comprising nitrogen ions, and exposing the silicon oxide surface to the plasma (col.6/ll.2-6; col.7/ll.42-62).

28. Regarding claims 25 and 26, Hagiwara (col.7/ll.62-67) teaches that nitriding the silicon oxide surface to incorporate nitrogen atoms into the surface may be accomplish by exposing the surface to an atmosphere containing nitrogen-atoms.

Hagiwara, however, fails to further specify a remote plasma nitridation (RPN) process or a decoupled plasma nitridation (DPN) process to perform the nitriding step.

Misium, on the other hand, teaches that RPN is an improved low-temperature method for creating a nitrided layer that is resistant to oxide etchants while Chou teaches that nitriding Hagiwara's silicon oxide surface by DPN avoid damages to the surface.

29. Regarding claim 27, Hagiwara/Misium/Chou shows most aspects of the instant invention (see paragraphs 23-28 above), except for the step of nitriding the silicon oxide surface resulting in a nitrided silicon oxide layer less than 3 nm thick.

Hagiwara (col.6/ll.11), however, shows that an illustrative thickness for such a layer falls between 5 to 10 nm. Although, the claimed thickness (< 3.0 nm) and the prior art thickness (5-10nm) do not overlap, it has been held that a *prima facie* case of obviousness exists where the claimed values and the prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties. It appears that the differences in thickness between Hagiwara and the claimed invention produce no change in the properties of the nitrided silicon oxide layer and therefore would have been obvious (*Titanium Metals Corp of America v. Banner*, 778 F.ed 775, 227 USPQ 773 (Fed. Cir. 1985)).

30. Claims 17, 20, and 28 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Misium and Chou.

31. Lin shows most aspects of the instant invention including a method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

- forming a first layer **120** comprising a silicon surface, the first layer providing a floating gate for the memory (see, *e.g.*, fig. 2A)
- nitriding the silicon surface of the first layer **120** to incorporate nitrogen atoms into the silicon surface (see, *e.g.*, fig. 2B)
- forming a first dielectric **143** at the nitrided surface, wherein forming the first dielectric **143** comprises forming silicon oxide at the nitrided surface (see, *e.g.*, fig. 2C)
- forming a conductive layer **150** separated from the nitrided surface from the nitrided surface by the first dielectric **143**, the conductive layer **150** providing a control gate for the memory

In addition, Lin (col.5/ll.54) teaches that nitriding the silicon surface of the first layer to incorporate nitrogen atoms into the surface may be accomplish by exposing the surface to an nitrogen treatment. Lin, however, fails to further specify a remote plasma nitridation (RPN) process or a decoupled plasma nitridation (DPN) process to perform the nitriding step.

Misium (col.2/ll.1-3), on the other hand, teaches that RPN is an improved low-temperature method for creating a nitrided layer that is resistant to oxide etchants, whereas Chou (col.5/ll.63-67) teaches that nitriding Hagiwara's silicon oxide surface by DPN avoid damages to the surface.

It would have been obvious at the time of the invention to one of ordinary skill in the art to nitride Lin's silicon oxide surface by remote plasma nitridation, as suggested by Misium, to lower the thermal budget of the process.

Alternatively, it would have been obvious at the time of the invention to one of ordinary skill in the art to nitride Lin's silicon oxide surface by DPN, as suggested by Chou, to avoid damaging the surface.

32. Regarding claim 20, Lin (col.4/ll.60) shows that forming the silicon oxide at the nitrided surface comprises forming the silicon oxide by thermal oxidation.

33. Regarding claim 28, Lin (col.4/ll.66) shows that nitriding the silicon surface results in forming at the silicon surface a layer of nitrided silicon less than 3 nm thick.

Response to Arguments

34. Applicant's arguments and/or comments with respect to claims 1-3, 7, and 10-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

36. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

37. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

39. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

40. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 438/257-267,514-534, 257/324	12/12/2002
Other Documentation:	12/12/2002
Electronic Database(s): EAST (USPAT, EPO, JPO)	12/12/2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800

Marcos D. Pizarro-Crespo
Patent Examiner
Art Unit 2814
703-308-6558
marcos.pizarro@uspto.gov

MDP/mdp
December 12, 2002